



## 5G/6G Research Projects at IIT Hyderabad

Date: 2<sup>nd</sup> June .2025

Applications are invited from the eligible candidates for the below positions from eligible candidates purely on ad hoc basis in the project: ROLLING ADVERTISEMENT

1.	Name of post	Project Officer Engineer 3
2.	Job Description	Responsibilities:
		Software/hardware design expert with B. Tech or M. Tech with an
		experience of 5 years'. The tasks performed are development of design,
		algorithms, and development/implementation of Layer 1,2,3 software. Also,
		development of system-level-simulation tools and development of RTL on
		FPGA boards and embedded software. Testing of developed software and
		FPGA based solutions with signal generation/analysis and protocol testers.
3	Essential	Also, mentoring the juniors Engineers. B Tech / B.E / MTech / ME / MS Master's/Bachelor's degree in Electrical/ Electronic
5	Qualification	Engineering, Computer Engineering, or equivalent practical experience
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5	Skills/Experience	Domain Knowledge on RTL Design, implementation, and integration for
	Required	FPGA based designs.
		• Experience with RTL coding using Verilog/System Verilog.
		• Proficiency in complete <b>FPGA design flow</b> .
		• Experience with protocols like <b>AXI4-stream</b> and <b>AXI4</b> .
		Development of analog RF front-end digital FPGA board
		Design & develop a L1/L2/L3 protocol stack

		<ul> <li>Contribute to software design, development, validation, and documentation to deliver high-quality products in the world of 5G</li> </ul>
5.	Consolidated Pay/ Per Month	1,50,000 INR
7.	Anticipated start date	01 <sup>st</sup> Jul 2025
8.	Tenure of employment	Contract period of 11 months. However, candidate can be reengaged for subsequent termsbased on his/her performance and requirement of the Department/Institute.
9.	Mode of selection	Test And Interview
10.	Selection Procedure:/ Mode of Application	<ol> <li>Interested applicants should apply online through the online google form Link :https://docs.google.com/forms/d/1wBOZ2dFh25vh2de5uue881LvX5VTDcEH uon966ApcUQ/edit</li> <li>The candidate will be shortlisted based on the eligibility criteria, academic record, and relevant experience and selected based on the performance in the written test/Interview.</li> <li>Date and Time of Interview: This will be intimated to shortlisted candidates via email.</li> <li>IIT Hyderabad reserves the right to alter the number of vacancies or keep it open till the deserving candidate is found.</li> <li>IIT Hyderabad reserves the right to close the recruitment procedure without selecting anybody, if none of the candidates are found suitable.</li> <li>Candidates with prior experience in relevant area will be given preference.</li> </ol>
11.	Contact	Candidate may contact: (Email: <u>srinivas.kvn@5g.iith.ac.in</u> / careers@5g.iith.ac.in

1.	Name of post	Senior Project Officers/ Engineer-4
2.	Job Description	Responsibilities: Software/hardware design expert with an experience of 7 years'. The tasks performed are design and algorithms development, reviewing the design and implementation. Also, development of system-level-simulation tools and development of RTL on FPGA boards and embedded software. Also, development of RTL on FPGA boards and embedded software, RF front-end digital FPGA board and embedded firmware. To do the field trails for the developed systems. Further, mentoring the juniors Engineers.
3	Essential Qualification	B Tech / B.E / MTech / ME / MS Master's/Bachelor's degree in Electrical/ Electronic Engineering, Computer Engineering, or equivalent practical experience
5	Skills/Experience Required	<ul> <li>Domain Knowledge on RTL Design, implementation, and integration for FPGA based designs.</li> <li>Experience with RTL coding using Verilog/System Verilog.</li> <li>Proficiency in complete FPGA design flow.</li> <li>Experience with protocols like AXI4-stream and AXI4.</li> <li>Development of analog RF front-end digital FPGA board</li> </ul>

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		Design & develop a L1/L2/L3 protocol stack
		<ul> <li>Contribute to software design, development, validation, and documentation to deliver high-quality products in the world of 5G</li> </ul>
		<ul> <li>Platform development with Xilinx Linux and Windriver linux and board- bring up</li> </ul>
		Very good in C and Embedded C programming
5.	Consolidated Pay/ Per Month	2,00,000 INR
7.	Anticipated start date	01 <sup>st</sup> Jul 2025
8.	Tenure of employment	Contract period of 11 months. However, candidate can be reengaged for subsequent termsbased on his/her performance and requirement of the Department/Institute.
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