Project Staff opportunities (Full time contract basis) at IITH with in the R&D project.

Number of positions: 1 no.

Key Responsibilities:

- Assist in designing and developing partial RTL code for digital logic blocks or modules using Verilog.
- Support synthesis of RTL code to gate-level netlists using industry-standard tools.
- Perform Place and Route (PnR) for gate-level netlists and contribute to optimization efforts.
- Run physical verification steps including DRC and LVS to ensure design compliance.
- Collaborate with senior team members to ensure successful integration of design modules into larger subsystems.
- Maintain well-documented and clean code that adheres to best practices and standards.

Required Skills:

- Experience writing partial RTL code in Verilog for digital modules.
- Understanding of digital design flow including synthesis and timing closure.
- Basic experience in Place and Route (PnR) for gate-level designs.
- Familiarity with physical verification tools and procedures (e.g., DRC, LVS).
- Good analytical and debugging skills.
- Ability to work in a team and communicate technical details clearly.

Preferred Tools: (Nice to have but not required)

- Synopsys Design Compiler, Cadence Innovus, Mentor Calibre, or similar tools.

Preferred Qualification:

- Bachelor's degree in Electronics and Communication Engineering, Electrical Engineering, or a related field.
- Minimum of 6 months hands-on experience in digital design using Verilog.

Salary: 25k to 40k per month.

Contract Period: 1 year and will be extended based on their performance and requirement.

Job Location: IIT Hyderabad, DARMIC LAB.

Joining Date:8th August 2025

How to apply: Kindly drop your latest resume at **parameshwari.p@ee.iith.ac.in** on or before 2nd August 2025.

Last date to receive CV is by 2nd August 2025.