

Applications are invited from the eligible candidates for the below positions from eligible candidates purely on ad hoc basis in the project

1.	Name of post	Senior Project Associate Engineer
2.	Job Description	Software/hardware design expert with B. Tech or M. Tech with an experience of 2-3 year's. The tasks performed are development of design and algorithms. Also, development of system-level-simulation tools and development of RTL on FPGA boards and embedded software.
3.	No. of post	02
4.	Essential Qualification	B tech / BE/ M tech /MCA/MSC/BSC ME / MS Master's Bachelor's degree Electrical /Electronic engineering, Computer engineering or Equivalent practical experience
5.	Skills /Experience Required	<ul style="list-style-type: none"> • Exp Level 2 to 3 Years • Domian Knowledge on RTL Design, implementation, and integrations for FPGA Designs. • Knowledge with RTL coding using Verilog/System Verilog. • Experience with protocols like AXI4-stream and AXI4. • Strong debugging capabilities at RTL simulation and FPGA Emulation.
6.	Consolidated Pay	Rs. 100,000 to 121,000
7.	Anticipated start date	01 st June 2025
8.	Tenure of employment	Contract period of 11 months. However, candidate can be reengaged for subsequent termsbased on his/her performance and requirement of the Department/Institute.
9.	Mode of selection	Test and interview
10.	Selection Procedure /Mode of application	<p>1 Interested applicant should apply online through the online google form link .</p> <p>https://docs.google.com/forms/d/1wBOZ2dFh25vh2de5uue881LvX5VTDcEHuon966ApcUQ/edit</p> <p>2.The candidate will be shortlisted based on the eligibility criteria, academic record, and relevant experience and selected based on the performance is the Witten interview.</p> <p>3 Date and time of interview: this will be intimated to shortlisted candidates via email.</p> <p>4 IIT Hyderabad reserves the right to alter the number of vacancies or keep it open till the deserving the right to close the recruitment procedure with out selecting anybody, if none of the candidates are found suitable .</p> <p>6. Candidates with prior experience in relevant areas will be given preference</p>

11.	Tentative date of interview	Date & Time will be informed through mail to shortlisted candidates
12.	Contact	Candidate may contact: (Email:Srinivas.kvn@5g.iith.ac.in) carrers@5g.iith.ac.in